

Table 2-2. Voltage Identification Definition

Processor Pins					V <sub>CC_MAX</sub>
VID4	VID3	VID2	VID1	VID0	
1	1	1	1	1	VRM output off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600

### 2.4.1 Phase Lock Loop (PLL) Power and Filter

V<sub>CCA</sub> and V<sub>CCIOPLL</sub> are power sources required by the PLL clock generators on the Pentium 4 processor on 0.13 micron process. Since these PLLs are analog, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system; it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V<sub>CC</sub>. A typical filter topology is shown in [Figure 2-2](#).

The AC low-pass requirements, with input at V<sub>CC</sub> and output measured across the capacitor (C<sub>A</sub> or C<sub>IO</sub> in [Figure 2-2](#)), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

Refer to the appropriate platform design guide for recommendations on implementing the filter.





**Table 4-1. Pin Listing by Pin Name**

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	C18	Power/Other	
VCC	C20	Power/Other	
VCC	C8	Power/Other	
VCC	D11	Power/Other	
VCC	D13	Power/Other	
VCC	D15	Power/Other	
VCC	D17	Power/Other	
VCC	D19	Power/Other	
VCC	D7	Power/Other	
VCC	D9	Power/Other	
VCC	E10	Power/Other	
VCC	E12	Power/Other	
VCC	E14	Power/Other	
VCC	E16	Power/Other	
VCC	E18	Power/Other	
VCC	E20	Power/Other	
VCC	E8	Power/Other	
VCC	F11	Power/Other	
VCC	F13	Power/Other	
VCC	F15	Power/Other	
VCC	F17	Power/Other	
VCC	F19	Power/Other	
VCC	F9	Power/Other	
VCCA	AD20	Power/Other	
VCCIOPLL	AE23	Power/Other	
VCC_SENSE	A5	Power/Other	Output
VCCVID	AF4	Power/Other	Input
VID0	AE5	Power/Other	Output
VID1	AE4	Power/Other	Output
VID2	AE3	Power/Other	Output
VID3	AE2	Power/Other	Output
VID4	AE1	Power/Other	Output
VSS	D10	Power/Other	
VSS	A11	Power/Other	
VSS	A13	Power/Other	
VSS	A15	Power/Other	
VSS	A17	Power/Other	
VSS	A19	Power/Other	
VSS	A21	Power/Other	
VSS	A24	Power/Other	
VSS	A26	Power/Other	
VSS	A3	Power/Other	
VSS	A9	Power/Other	
VSS	AA1	Power/Other	

**Table 4-1. Pin Listing by Pin Name**

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AA11	Power/Other	
VSS	AA13	Power/Other	
VSS	AA15	Power/Other	
VSS	AA17	Power/Other	
VSS	AA19	Power/Other	
VSS	AA23	Power/Other	
VSS	AA26	Power/Other	
VSS	AA4	Power/Other	
VSS	AA7	Power/Other	
VSS	AA9	Power/Other	
VSS	AB10	Power/Other	
VSS	AB12	Power/Other	
VSS	AB14	Power/Other	
VSS	AB16	Power/Other	
VSS	AB18	Power/Other	
VSS	AB20	Power/Other	
VSS	AB21	Power/Other	
VSS	AB24	Power/Other	
VSS	AB3	Power/Other	
VSS	AB6	Power/Other	
VSS	AB8	Power/Other	
VSS	AC11	Power/Other	
VSS	AC13	Power/Other	
VSS	AC15	Power/Other	
VSS	AC17	Power/Other	
VSS	AC19	Power/Other	
VSS	AC2	Power/Other	
VSS	AC22	Power/Other	
VSS	AC25	Power/Other	
VSS	AC5	Power/Other	
VSS	AC7	Power/Other	
VSS	AC9	Power/Other	
VSS	AD1	Power/Other	
VSS	AD10	Power/Other	
VSS	AD12	Power/Other	
VSS	AD14	Power/Other	
VSS	AD16	Power/Other	
VSS	AD18	Power/Other	
VSS	AD21	Power/Other	
VSS	AD23	Power/Other	
VSS	AD4	Power/Other	
VSS	AD8	Power/Other	
VSS	AE11	Power/Other	
VSS	AE13	Power/Other	